In the Specification

Please amend the applicants' specification as indicated below:

Page 11, add the following after the 1st Paragraph

Figure 17 is an electrical schematic of a g_{ds} compensated, multi-level output driver with current control circuitry.

Figure 18 is an electrical schematic of a circuit for calibrating a g_{ds} compensated output driver with current control circuitry.

Figures 19A and 19B are a flowchart of a method for calibrating the current control circuitry using the setup of Figure 18 for the output driver shown in FIG. 17.

Page 31, add the following between the 2nd and 3rd Paragraphs

In Figure 17, a 4-PAM output driver corrects the g_{ds} distortion and provides current control. As described above, the signals A, B and C preferably determine the output voltage or symbol in accordance with the gray-coded binary signaling shown in Table 2, above. In addition, three sets of current control calibration bits, CC, CCB and CCC, respectively determine the amount of current supplied by the output driver for various combinations of A, B and C. The first set of control bits CC provides primary current control, while the second and third sets of current control bits, CCB and CCC, respectively, fine tune the amount of current. The first set of current control bits CC has N bits; the second set of current control bits CCB has n1 bits; and the third set of current control bits CCC has n2 bits. In one embodiment, the relationship between the number of current control bits is as follows:

$$n1 \leq n2 < N.$$

There may be different relationships between N, n1 and n2 in alternative embodiments.

Each of the A, B and C signals is associated with a current drive block 1740 to drive a predetermined amount of current associated with the symbol. Each current drive block 1740 includes one or more sets of stacked transistor pairs 1742 that are associated

with each set of current control bits for that current driver block 1740. For example, the current drive block 1740-1 that drives the A signal receives current control bits CC. The current drive block 1740-2 that drives the B signal receives current control bits CC and CCB. The amount of current supplied by current drive block 1740-2 is adjusted for g_{ds} distortion using the CCB bits. The current drive block 1740-3 that drives the C signal receives current control bits CC and CCC. The amount of current supplied by current drive block 1740-3 is adjusted for g_{ds} distortion using the CCC bits.

As shown in Figure 18, a current control calibration circuit 1850 determines the settings for the current control bits CC, CCB and CCC by selecting a current control reference voltage, V_{REF}, and comparing the current control reference voltage, V_{REF}, to a voltage at a mid-point between two calibration output voltages, V_{OUT}-1 and V_{OUT}-2. The current calibration circuit 1850 determines settings for each of the sets of current control bits CC, CCB and CCC for each 4-PAM output voltage such that V_{OUT}-1 and V_{OUT}-2 provide each adjacent pair of voltage levels to the circuit.

A multiplexer 1852 receives the three 4-PAM reference voltages V_{REFHI}, V_{REFM} and V_{REFLO}. A select reference voltage signal, SelRef, selects one of the referenced voltages as the selected current control reference voltage, V_{REF}. A comparator 1854 compares the selected current control reference voltage V_{REF} to a mid-point voltage V_X and generates a comparison signal.

To generate the mid-point V_X, output driver 1 1856 sinks a first amount of current to provide the first output voltage V_{OUT}-1 and output diver 2 1858 sinks a second amount of current to provide the second output voltage V_{OUT}-2. Two passgate pairs 1860 and 1862, in response to a current control enable and its complementary signal, act as a resistor divider to provide the midpoint voltage, V_X, between the first output voltage, V_{OUT}-1, and the second output voltage, V_{OUT}-2.

A state machine 1864 includes first, second and third counters, 1866-1, 1866-2 and 1866-3 that provide the first, second and third sets of current control bits, CC, CCB and CCC, respectively. If the comparison signal indicates that the midpoint signal V_X is greater than the reference voltage V_{REF}, the state machine 1864 increments an associated set of current control bits by one to increase the amount of current that is sunk by the output driver, thereby decreasing the midpoint voltage. If the midpoint voltage signal V_X

is less than the current control reference voltage, V_{REF}, the state machine 1864 decrements the associated current control bits by one, thereby increasing the midpoint voltage.

In one embodiment, the current control bits are calibrated during a power-up sequence. The theory of operation for calibrating the current control bits is as follows. The first set of current control bits CC provide the primary amount of current control for each current control block 1740 (Figure 17). To compensate for g_{ds} distortion, the CCB and CCC current control bits fine tune the amount of current associated with the Gray-coded "11" and "10" signals, respectively. The current control bits are calibrated in the following order: CC, CCB, and then CCC.

The first and main set of current control bits CC are set using the voltage differences between the "00" and "01" symbols. The first set of current control bits CC are set to provide an amount of current to provide the output voltage for the "01" symbol such that V_{REFHI} is placed at the midpoint between the output voltage for the "00" symbol and the output voltage for the "01" symbol.

Because of g_{ds} distortion, without compensation, the voltage difference between the "01" symbol and the "11" symbol is less than the voltage difference between the "00" symbol and the "01" symbol. To compensate for the g_{ds} distortion, the output voltage for the "11" symbol is decreased by increasing the amount of current sunk by the output driver. The second set of current control bits CCB are set to increase the current sunk by the output driver such that the output voltage becomes equal to the desired voltage level when the midpoint voltage between output voltage for the "01" and "11" is equal to V_{REFM}.

Finally, the third set of current control bits CCC is adjusted such that the midpoint voltage between output voltage for the "11" and "10" is equal to V_{REFL}.

Referring to Figures 18, 19A, and 19B, the operation of the circuit 1850 including the state machine 1864 will be described. The flowchart of Figures 19A and 19B uses gray coded output voltages. In step 1970, the current control enable signal (ccen) and its complement (ccenb) are set to activate the passgate pairs 1860 and 1862 and output the midpoint voltage V_X, described above.

Three major blocks of steps 1972, 1974 and 1976 set the current control bits, CC,

CCB and CCC, respectively.

In block 1972, step 1978 sets the initial conditions for determining the settings for the first set of current control bits CC. The state machine 1864 outputs the select reference voltage signal (SelRef) which causes the multiplexer 1854 to output the reference voltage V_{REFHI} to the comparator 1854. A "00" symbol is supplied to output driver 1 1856 by outputting multi-PAM bit selection signals A1, B1 and C1 with values of zero. A "01" symbol is supplied to output driver 2 1858 by outputting multi-PAM bit selection signals A2 with a value of one, and B2 and C2 with a value of zero. The initial state of the first, second and third current control bits is as follows:

CC={1 0 0 . . . 0};

CCB={1 0 0 . . . 0}; and

ti CCC={1 0 0 . . . 0}.

The current control bits are initially set such that the stacked transistor pair sinking the most current will be activated.

In step 1980, the output drivers 1 and 2 output the voltages corresponding to the symbols "00" (the V_{TERM} reference) and "01" (the drive level under calibration) and the midpoint voltage V_X is generated. In step 1982, the comparator 1854 compares the midpoint voltage V_X to the selected reference voltage V_{REFHI}. When the midpoint voltage is within one least significant bit of the reference voltage V_{REFHI}, the first set of current control bits have the proper setting. The state machine 1864 determines that the midpoint voltage V_X is within one least significant bit of the reference voltage V_{REFHI} when the current control bits begin to dither between two settings. In other words, the output of the comparator will alternate between a zero and a one.

In step 1984, when the midpoint voltage V_X is not within one least significant bit of the reference voltage V_{REFHI}, the state machine 1864 augments the first set of current control bits depending on the result of the comparison. The term "augment" is used to indicate either incrementing or decrementing the current control bits. The process proceeds to step 1980.

If, in step 1982, the state machine 1864 determines that the midpoint voltage V_X is within one least significant bit of the reference voltage, the process proceeds to step 1986 to calibrate the second set of current control bits, CCB.

In step 1986, the initial conditions for calibrating the second set of current control bits CCB are set. The state machine 1864 outputs the select reference voltage signal (SelRef) which causes the multiplexer 1854 to output the reference voltage V_{REFM} to the comparator 1854. A "01" symbol is supplied to output driver 1 1856 by outputting multi-PAM bit selection signals A1 with a value of one, and B1 and C1 with values of zero. A "11" symbol is supplied to output driver 2 1858 by outputting multi-PAM bit selection signals A2 and B2 with a value of one, and C2 with a value of zero. The state of the first set of current control signals CC remains unchanged. The initial state of the second and third sets of current control bits, CCB and CCC, respectively, is as follows:

CCB={1 0 0 . . . 0};

CCC={1 0 0 . . . 0}.

In step 1988, the output drivers 1 1856 and 2 1858 output the voltages corresponding to the symbols "01" (the level calibrated in step 1072) and "11" (the level now under calibration), and the passgate pairs 1860 and 1862 output the midpoint voltage V_X. In step 1990, the comparator 1854 compares the midpoint voltage V_X to the selected reference voltage V_{REFM}. When the midpoint voltage is not within one least significant bit of the reference voltage V_{REFM}, as described above with respect to V_{REFHI}, in step 1992, the state machine 1864 augments the second set of current control bits CCB by one and the process repeats at step 1986.

When the midpoint voltage is within one least significant bit of the reference voltage V_{REFM}, as described above with respect to V_{REFHI}, the second set of current control bits CCB have the proper setting and the process proceeds to step 1994 to calibrate the third set of current control bits, CCC.

In step 1994, the initial conditions for calibrating the third set of current control bits CCC are set. The state machine 1864 outputs the select reference voltage signal (SelRef), which causes the multiplexer 1854 to output the reference voltage V_{REFLO} to comparator 1854. A "11" symbol (calibrated in step 1074) is supplied to output driver 1 1856 by outputting multi-PAM bit selection signals A1 and B1 with a value of one, and C1 with a value of zero. A "10" symbol (the level now under calibration) is supplied to output driver 2 1858 by outputting multi-PAM bit selection signals A2, B2 and C2 with a value of one. The state of the first and second sets of current control signals CC and

CCB, respectively, remains unchanged. The initial state of the third set of current control bits CCC is as follows:

$$CCC=\{1\ 0\ 0\ \ldots\ 0\}.$$

In step 1996, the output drivers 1 1856 and 2 1858 output the voltages corresponding to the symbols "11" and "10" and the passgate pairs 1860 and 1862 output the midpoint voltage V_X. In step 1998, the comparator 1854 compares the midpoint voltage V_X to the selected reference voltage V_{REFLO}. When the midpoint voltage is not within one least significant bit of the reference voltage V_{REFLO}, as described above with respect to V_{REFHI}, in step 1999, the state machine 1864 augments the third set of current control bits CCC by one and the process repeats at step 1994.

In step 1998, when the midpoint voltage is within one least significant bit of the reference voltage V_{REFLO}, the appropriate settings for the first, second and third sets of current control bits, CC, CCB and CCC respectively are determined and the calibration is complete.

For the foregoing embodiment, a sequential search is described: starting at an initial value and augmenting. It should be emphasized, however, that alternative search techniques known to those skilled in the art may be used. For example, without limiting the foregoing, successive approximation using a binary search may be used. As a further alternative, a direct flash conversion may be used. This alternative is less desirable, however, because it is hardware intensive.